REMARKS

Claims 7-26 are pending in the current application. Claims 7-26 were previously presented in a Preliminary Amendment. Claims 1-6 were previously canceled. Claim 7 is currently amended.

The Office Action indicates that claims 7-26 are rejected.

Applicants respectfully request reconsideration of the application in view of the foregoing amendments and the remarks appearing below.

Rejections Under 35 U.S.C. §112

Claim 7 stands rejected under 35 U.S.C. §112(2) as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention. In particular, the U.S. Patent and Trademark Office (USPTO) asserts that use of the phrase "means for allocating" is ambiguous because it is not clearly defined in the specification, when used in "means for allocating redundancy resources of the memory system." Applicants respectfully disagree.

The USPTO's attention is directed to Applicants' language in the following portions of the application: (1) ¶0008, last line "the finite state machine allocating redundancy resources of the memory system according to the decision algorithm;" (2) ¶0009 last line "...according to a decision algorithm;" (3) ¶0021 "A higher weight indicates more replacement efficiency, so this weight will be taken into account when determining how to repair the failing addresses;" (4) ¶0022 "When the highest weighted row is assigned to FME 22 that row and column address pair are replaced by a redundant element, so all fails on that row are fixed and that column fail on that row is also repaired. This results in all fails with the same row address simultaneously marked invalid, i.e., cleared from TME 30, and any fails with matching column addresses have their weights reduced by one;" and (5) Fig. 2, illustrating the algorithm.

Applicants recognize that "means for" type limitations under 35 U.S.C. § 112, sixth paragraph, require structure corresponding to the means to be present in the current specification. Applicants respectfully submit that this required structure is indeed inherently present in the current application. This is so because, as mentioned above, Applicants specifically mention that a finite state machine is provided for allocating redundancy resources. While Applicants realize that a finite state machine does not necessarily denote any particular structure, those having

ordinary skill in the art will immediately recognize that in order to instantiate the finite state machine of the inventive redundancy architecture into real world practice, they will have to implement the finite state machine, and its attendant decision algorithm, into a physical structure, such as an integrated circuit chip or portion thereof. As those skilled in the art will readily recognize, the finite state machine and decision algorithm can be implemented in a structure using any suitable software or hardware techniques, or a combination thereof. Consequently, it is Applicants' position that the hardware and/or hardware/software combination supporting such an instantiation of the finite state machine and decision algorithm provides the proper support for the "means for" limitation of claim 7.

Nonetheless, Applicants have amended independent claim 7 to clarify the "means for allocating" phrase to read "means for assigning ones of the failed row and column addresses having weights greater than a threshold for permanent storage in said first or second memory element." Although this language is different from the language addressed by the USPTO in the present rejection, Applicants respectfully submit that the issue is the same. That is, those skilled in the art would readily understand the structure necessary to implement a finite state machine that contains a decision algorithm for assigning ones of failed row and column addresses having weights greater than a threshold for permanent storage in first and second (row and column) memory elements.

For at least the foregoing reasons, Applicants believe that claim 7, and claims 8-13 that depend therefrom, are more clearly allowable. Therefore, Applicants respectfully request withdrawal of the present rejection.

Rejections under 35 U.S.C. §103

Irrinki et al./Kawagoe

Claims 7, 9-13, 14, 16-23, 25 and 26 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,987,632 to Irrinki et al. in view of U.S. Patent No. 6,243,307 to Kawagoe. Applicants respectfully disagree.

Irrinki et al. disclose a two-pass test for making row and column repairs to a memory using redundant elements. The first pass involves testing a memory element under worst case conditions and, if a failure is seen, marking it as permanently failing. The second pass is performed under more normal operating conditions and involves rediscovering the memory element marked as failing in the first pass and mapping a redundant memory element as a

replacement (along with repairing/mapping redundant elements to repair any newly found fails). Importantly, Irrinki et al. are completely silent on the use of any sort of weighting scheme and a third memory element for accumulating failed row and column addresses and associated assigned weights.

Kawagoe discloses a dynamic random access memory 1000 (FIG. 1) that includes a built-in self-test (BIST) circuit 2000 (FIGS. 1 and 2). BIST circuit 2000 includes an address replacement determinator 3000 (FIGS. 2 and 3) that, in the explicit example provided for a scheme having two redundant columns and two redundant rows, allows for a parallel determination to be made as to which of the six combinational cases of possible replacement configurations (col. 10, lines 10-19) can satisfy a given set of failed memory locations. As seen in FIG. 3 of the Kawagoe patent, to facilitate this functionality for six combinational cases address replacement determinator 3000 has six row address storage units RM1-6, six column address storage units CM1-6, and six replacement determination units 3100.1-.6. Each of the six replacement determination units 3100.1-.6 corresponds to a respective one of the six combinational cases illustrated in col. 10, lines 14-19. Again, this configuration allows address replacement determinator 3000 to analyze all six combination cases in parallel with one another, i.e., simultaneously.

Importantly, Kawagoe is completely silent on using any sort of weighting scheme for determining how to allocate redundant memory elements. All Kawagoe teaches is the determining which of the six combinational cases will bring about a repair of all the failing memory elements in a particular set of such elements. Applicants respectfully submit that the determining which of a finite set of solutions is correct cannot reasonably be considered a type of weighting.

Turning now to the rejected claims, independent claim 7, as amended, requires the limitations of "a third memory element for accumulating failed row and column addresses transmitted from said BIST and assigning each of the failed row and column addresses a particular weight value based on the number of the failed row and column addresses already accumulated in said third memory element and the relative locations of the failed row and column addresses within the memory system," and "means for assigning ones of the failed row and column addresses having weights greater than a threshold for permanent storage in the first or second memory element." Applicants respectfully submit that neither the Irrinki et al. patent

nor the Kawagoe patent disclose or suggest either of these limitations. Again, neither of these patents can be fairly read to disclose or suggest any sort of weighting feature and, therefore, cannot be said to disclose a third memory element that assigns weights to addresses stored therein, nor a means for assigning ones of such stored addresses to first and second memory elements as a function of the assigned weights.

For at least the foregoing reasons, Applicants respectfully submit that the applied combination of the Irrinki et al. and Kawagoe patents cannot render obvious independent claim 7, nor claims 9-13 that depend therefrom.

Regarding independent claim 14, this claim requires among other things the limitations of "assigning failed row and column addresses accumulated in step b a particular weight value based on the number of like addresses already accumulated." Applicants respectfully submit that neither the Irrinki et al. patent nor the Kawagoe patent disclose or suggest this limitation. Again, neither of these patents can be fairly read to disclose or suggest any sort of weight assignment related to failed addresses and, therefore, cannot be said to disclose a third memory element that assigns weights to first and second memory elements as a function of the assigned weights.

For at least the foregoing reasons, Applicants respectfully submit that the applied combination of the Irrinki et al. and Kawagoe patents cannot render obvious independent claim 14, nor claims 16-20 that depend therefrom.

Regarding independent claim 21, this claim requires among other things the limitations of "a third memory element for accumulating said row and column addresses identified by said BIST and assigning them a particular weight value based upon the number of like addresses already accumulated in said third memory element and their relative locations within the memory system." Applicants respectfully submit that neither the Irrinki et al. patent nor the Kawagoe patent disclose or suggest this limitation. Again, neither of these patents can be fairly read to disclose or suggest any sort of weight assignment related to failed addresses and, therefore, cannot be said to disclose a third memory element that assigns weights to first and second memory elements as a function of the assigned weights.

For at least the foregoing reasons, Applicants respectfully submit that the applied combination of the Irrinki et al. and Kawagoe patents cannot render obvious independent claim 21, nor claims 22-26 that depend therefrom.

For at least the foregoing reasons, Applicants respectfully request withdrawal of the present rejection.

Irrinki et al./Kawagoe/Ohtani et al.

Claims 8, 15 and 24 stand rejected under 35 U.S.C. §103(a) as being unpatentable over a combination of the Irrinki et al. and Kawagoe patents, discussed above, and further in view of U.S. Patent Application Publication No. 2002/0196683 to Ohtani et al. Applicants respectfully disagree.

The pertinent disclosures of the Irrinki et al. and Kawagoe patents are as described above relative to the obviousness-type rejection in view of the combination of those patents.

Ohtani et al. disclose memory that includes content-addressable memory cells. Ohtani et al. also address a deficiency in the redundancy allocation of the Kawagoe patent when the redundant memory domain has multiple sub-memory cell arrays that share a single row sub-memory address list but have separate and distinct column sub-memory address lists. The Ohtani et al. publication's proposed solution involves completing a Kawagoe-style combinatorial repair allocation with a primary replacement determining unit for each sub-memory cell array, followed by a secondary replacement determining unit that allocates redundant memory where the repairs are common to each primary replacement determining units (paragraph 0082 of the Otahni et al. publication). Importantly, Otahni et al. do not disclose the use of any sort of weighting scheme or a third memory element for accumulating failed row and column addresses with associated assigned weights.

Because the Otahni et al. publication does not add anything material to the Irrinki et al./Kawagoe combination discussed in the previous section other than the concept of content-addressable memory cells, the reasons set forth above for the impropriety of the Irrinki et al./Kawagoe rejection of independent claims 7, 14 and 21 are likewise applicable to the present rejection. That is, because the applied combination of Irrinki et al., Kawagoe and Ohtani et al. references is silent on use of an assigned weighting scheme, Applicants respectfully submit that this combination cannot render obvious claims 8, 15 and 24 which depend from, respectively, independent claims 7, 14 and 21 addressed in the previous section.

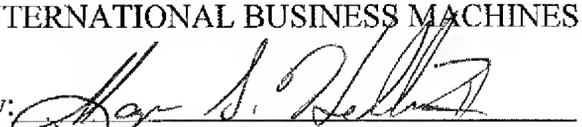
For at least the foregoing reasons, Applicants respectfully request withdrawal of the present rejection.

CONCLUSION

In view of the foregoing, Applicants respectfully submit that claim 7-26, as amended, are in condition for allowance. If any issues remain, the Examiner is encouraged to call the undersigned attorney at the number listed below.

Respectfully submitted,

INTERNATIONAL BUSINESS MACHINES CORP.

By: 

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